(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number
WO 2004/010586 A3

(51) International Patent Classification[7]: H03M 1/14

(21) International Application Number: PCT/IB2003/003027

(22) International Filing Date: 8 July 2003 (08.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0216897.9 20 July 2002 (20.07.2002) GB

(71) Applicant *(for all designated States except US)*: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: HUGHES, John, B. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(74) Agent: WILLIAMSON, Paul, L.; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

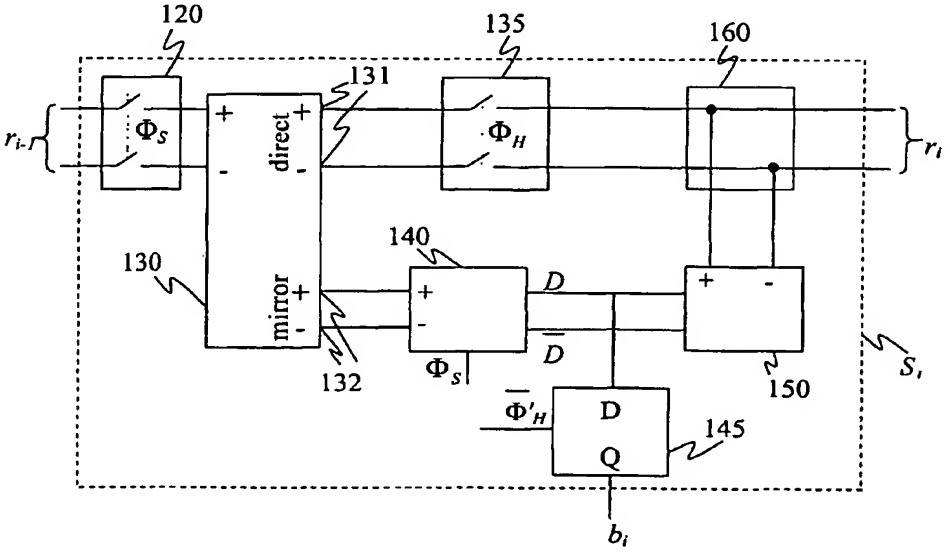
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: SWITCHED-CURRENT ANALOGUE-TO-DIGITAL CONVERTER



(57) Abstract: A current mode analogue-to-digital converter uses a conversion stage which operates using a two-phase clock and which requires the input signal to be present during only one of the phases. A sample-and-hold circuit (120, 130, 135) samples the input signal during the first clock phase and during the second clock phase a quantised bit value is generated from a mirror of the held input current by a kickback-free comparator circuit (140). Also during the second clock phase a residue is generated using the quantised value and a non-mirrored version of the held input current. Optionally, two comparator circuits (140, 140") may be used to provide two-level quantisation, enabling errors introduced by the current mirror to be corrected by a Redundant Signed Digit algorithm. Two pipelines of conversion stages ($S_{i'}$, $S_{i''}$) can be multiplexed to double the conversion rate.

WO 2004/010586 A3

(88) Date of publication of the international search report:
21 May 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/IB 03/03027

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M1/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 313 780 B1 (HUGHES JOHN B ET AL) 6 November 2001 (2001-11-06) ---	
A	SROWIK R ET AL: "Low-power class AB current memory cell" , ELECTRONICS LETTERS, IEE STEVENAGE, GB, VOL. 35, NR. 23, PAGE(S) 2014-2015 XP006012931 ISSN: 0013-5194 --- -/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 February 2004	16/02/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Oliveira, J.

2

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/IB 03/03027

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	BRACEY M ET AL: "A 70MS/S 8-BIT DIFFERENTIAL SWITCHED-CURRENT CMOS A/D CONVERTER USING PARALLEL INTERLEAVED PIPELINES" , 1995 IEEE TENCON. IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI. HONG KONG, NOV. 6 - 10, 1995, IEEE REGION TEN INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI.(TENCON), NEW YORK, IEEE, US, PAGE(S) 143-146 XP000585762 ISBN: 0-7803-2625-3	

2

INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/IB 03/03027

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6313780 B1	06-11-2001	WO 0019614 A2	06-04-2000
		EP 1046231 A2	25-10-2000
		JP 2002526964 T	20-08-2002